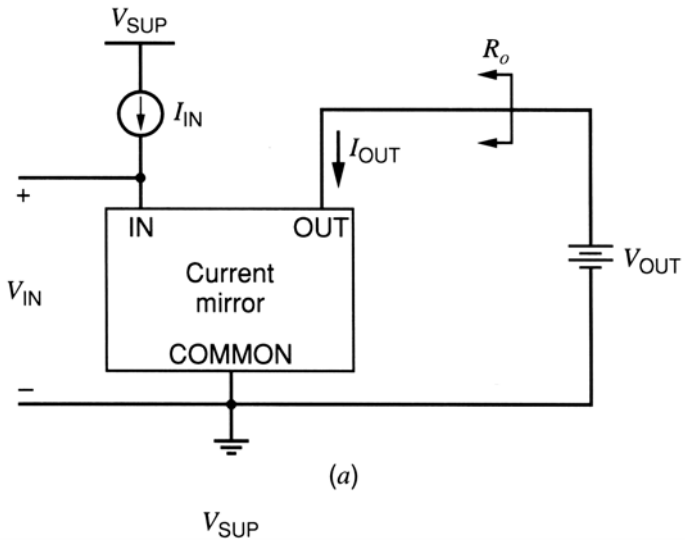
Current Mirrors/Active Loads

Overview

- Current mirrors
- Active loads
- Voltage and current references

Current Mirrors

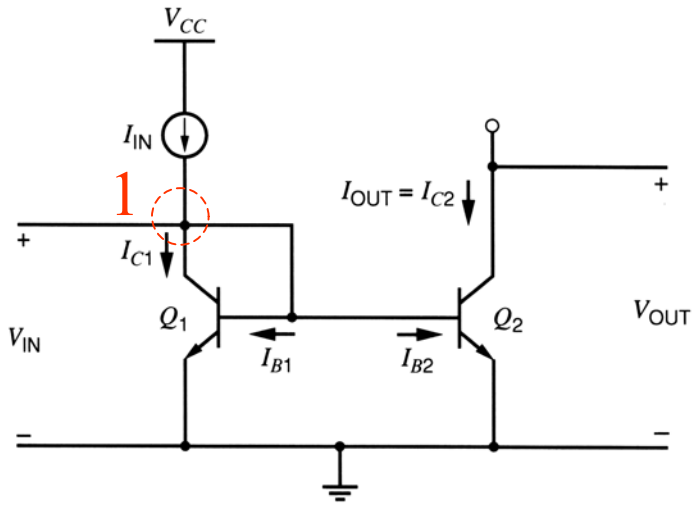
- Desired features
  - Generate an output current equal to input current multiplied by desired current gain factor
  - Current gain is independent of input frequency
  - Output current independent of output voltage to common node
  - Input voltage to be zero to let a larger voltage appear across input current source
- In reality
  - Variation of output current with voltage change at output => increase output resistance in small signal
  - Deviation of current gain from ideal number
  - Vin is a finite number that need to be minimized



Simple Bipolar Current Mirror

- Simplest form of current mirror
- Operation
  - Diode connecting base to collector in Q1, operation in active mode
  - $V_{be1}=V_{be2}$

$$I_{C2}=\frac{I_{S2}}{I_{S1}}I_{C1}$$



  - Writing KCL for point 1

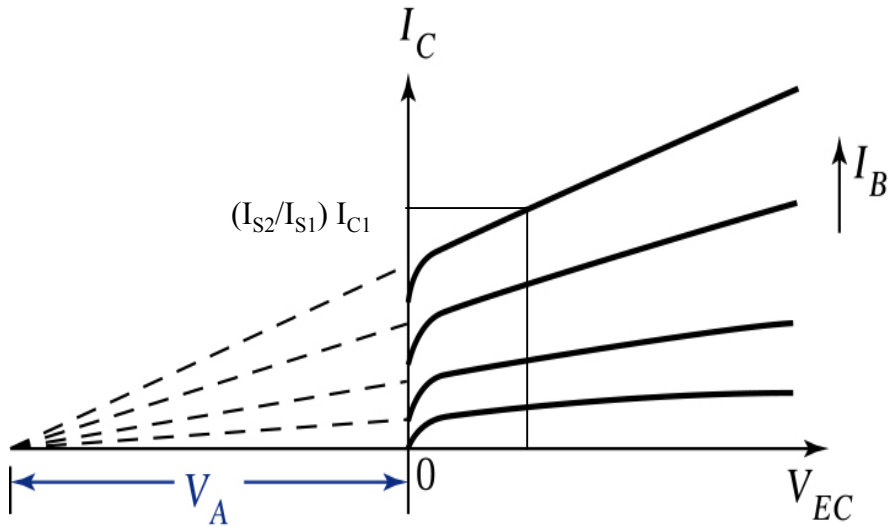
$$I_{IN}-I_{C1}-\frac{I_{C1}}{\beta_F}-\frac{I_{C2}}{\beta_F}=0$$

  - Current gain defined by saturation current => emitter areas
  - Systematic error source
    - ☛ β_F

$$I_{OUT}=\frac{I_{S2}}{I_{S1}}I_{IN}\left(\frac{1}{1+\frac{1+I_{S2}/I_{S1}}{\beta_F}}\right)\xrightarrow{I_{S1}=I_{S2}}I_{Out}\sim I_{IN}$$

Simple Bipolar Current Mirror (cont.)

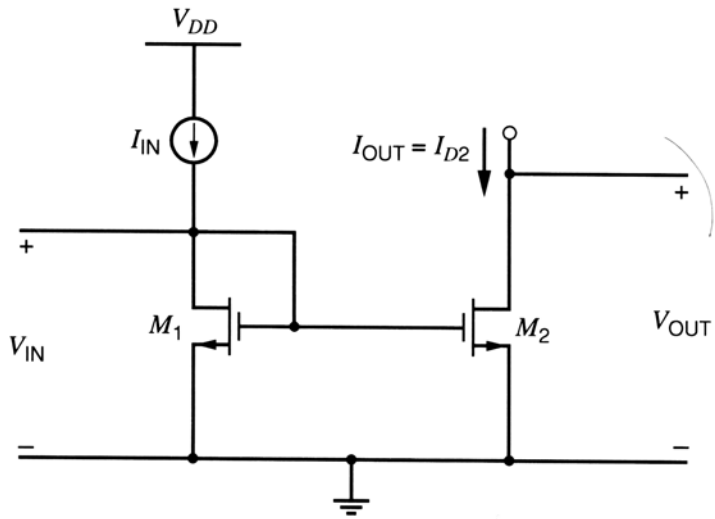
- In case of finite output resistance, change of output voltage changes I_{C2}
- Output current



$$I_{OUT} = \frac{I_{S2}}{I_{S1}} I_{C1}\left(1+\frac{V_{CE2}-V_{CE1}}{V_A}\right) = \frac{\frac{I_{S2}}{I_{S1}} I_{IN}\left(1+\frac{V_{CE2}-V_{CE1}}{V_A}\right)}{1+\frac{1+I_{S2}/I_{S1}}{\beta_F}}$$

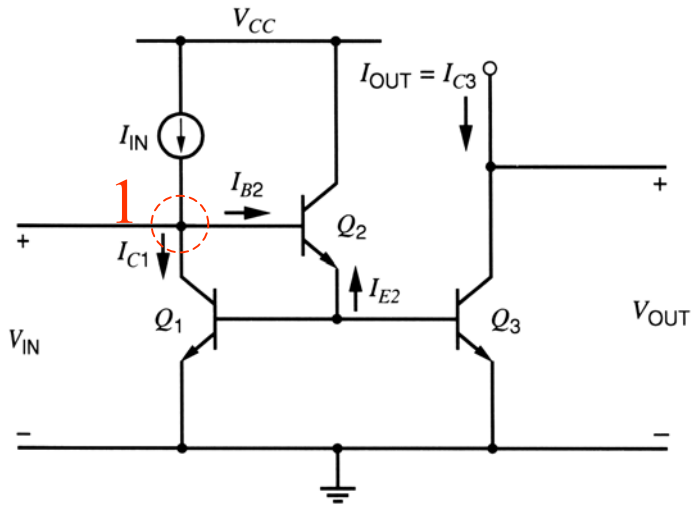
Simple MOSFET Current Mirror

- Simple current source
- Operation
  - M1, diode connected, operates in saturation
  - $V_{gs2}=V_{gs1}$
  - The current gain is defined by device sizes
  - Error source



Beta Helper

- Adding another transistor to reduce the β_f source of error
  - Common for PNP that has lower β_f
- Features
  - Does not change output resistance or output voltage from simple bipolar current mirror
  - Increases the input voltage by another base-emitter voltage
  - Can be used for multiple output current sources



If Q_1 & Q_3 identical $\Rightarrow$ $$I_{OUT} = I_{IN}\left(1 - \frac{2}{\beta_F(\beta_F + 1)}\right)$$

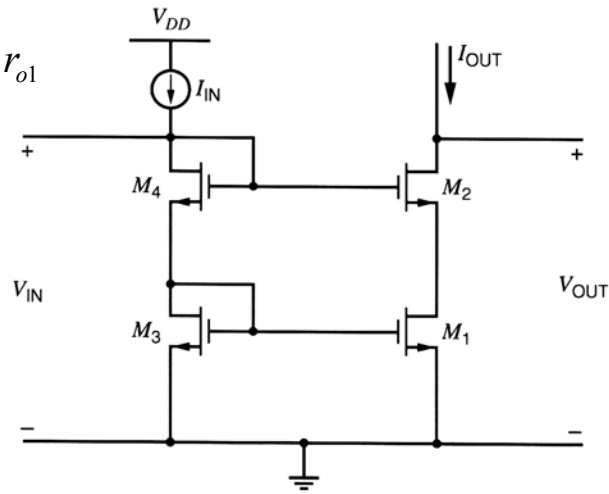
Cascode Current Mirror Simple case

- Achieves very high output gain
  - Each cascode stage increases the output resistance by $(1+g_m r_o)$
- Minimum input voltage:
  - For each stage, we add one (V_t+V_{ov}) to this minimum
    - Challenge for low voltage design
- Minimum output voltage:
  - So V_{DS1} is a threshold voltage more than it needs to be

$$R_o = r_{o2}\left[1+\left(g_{m2}+g_{mb2}\right)r_{o1}\right]+r_{o1}$$

$$V_{IN(\min)} = 2V_t + 2V_{ov}$$

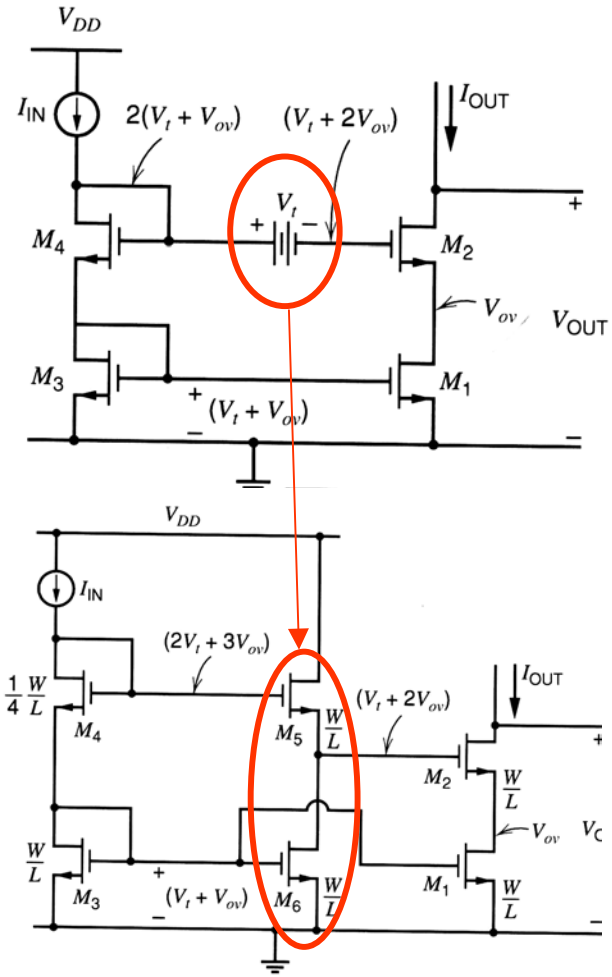
$$V_{Out(\min)} = V_t + 2V_{ov}$$



Cascode Current Mirror Improved Voltage Swing

- In order to improve the output swing, we need to voltage shift the gate voltage of M2
  - In case we use same transistors for all the devices => V_{DS1}=0
  - So we need to find optimum dimensions to give V_{DS1}=V_{ov}
- Output resistance is similar to simple cascode
- The input voltage is worsened
- The systematic gain error worsened, since M1 & M3 form a current mirror with unequal drain-source voltages

$$\varepsilon = \frac{V_{DS1} - V_{DS3}}{V_A} \approx \frac{V_{ov1} - (V_{ov1} + V_t)}{V_A} = -\frac{V_t}{V_A}$$



Cascode Current Mirror
Sooch Cascode

- To improve on mismatch and some power consumption, we could fold the level shift into one transistor
- The output resistance:

$$R_o = r_{o2}\left[1+\left(g_{m2}+g_{mb2}\right)r_{o1}\right]+r_{o1}$$

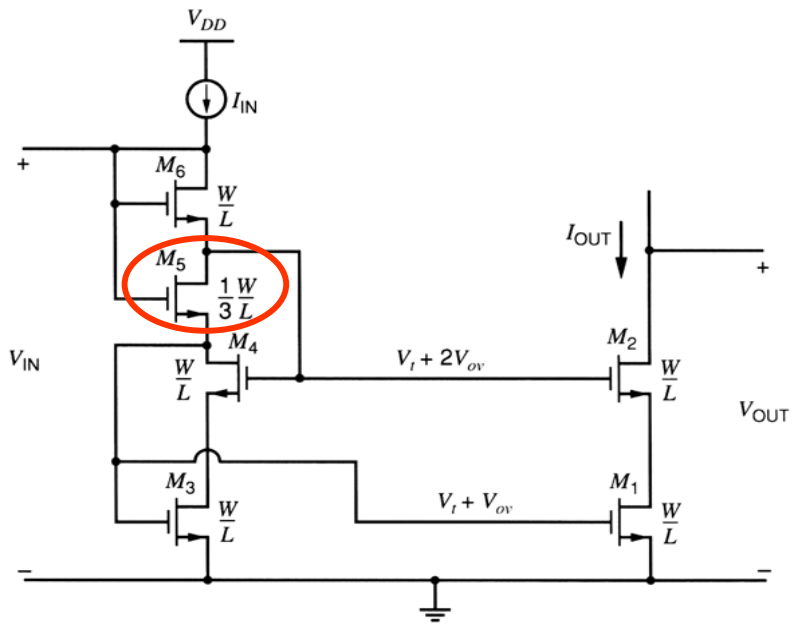
- Minimum input voltage:

$$V_{IN(\min)} = 2V_t + 3V_{ov}$$

- Minimum output voltage:

$$V_{OUT(\min)} \approx V_t + 2V_{ov}$$

- M4 ensures Q1 & Q3 have same VDS => systematic gain error goes to zero



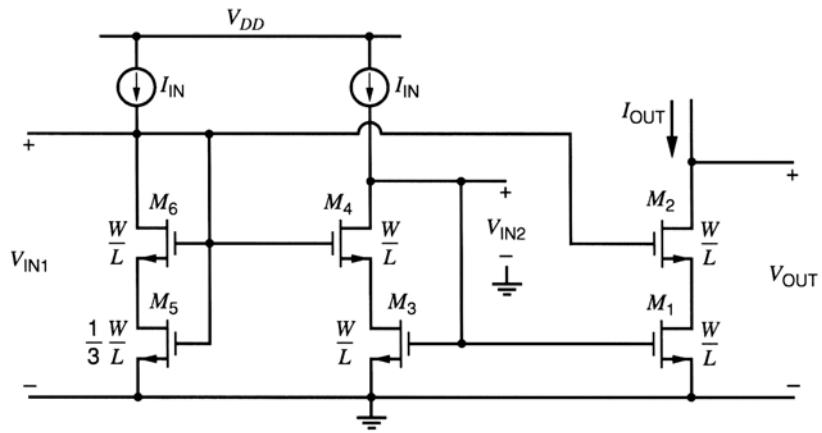
Cascode Current Mirror
Low Voltage Cascode

- For many low voltage applications, it is important to reduce the input voltage of cascode; this can be achieved by splitting the input branches
- Two input voltages need to satisfy:

$$V_{IN1(\min)} = V_t + 2V_{ov}$$

$$V_{IN2(\min)} = V_t + V_{ov}$$

- Therefore can be achieved with lower supply voltages



Wilson Current Source

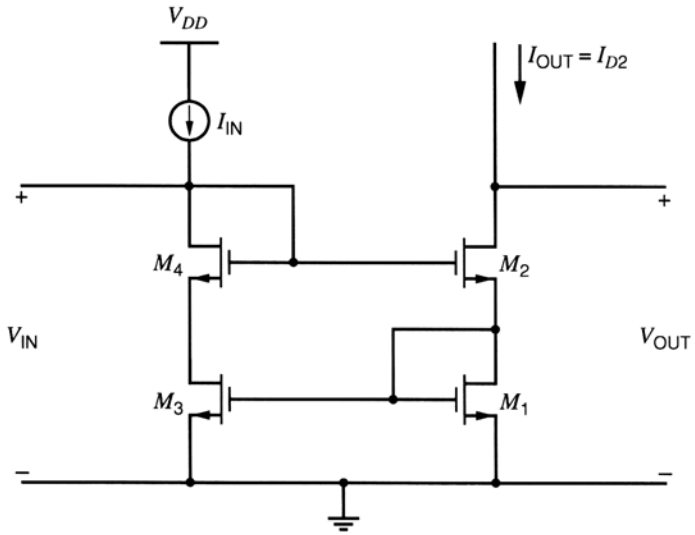
- Goal is reducing the systematic error and achieve large output resistance
- The output resistance is given by: $R_o = r_{o2}\left[2 + g_{m2}r_{o3}\right]$
- Minimum input voltage:

$$V_{IN(\min)} = 2V_t + 2V_{ov}$$

- Minimum output voltage:

$$V_{OUT(\min)} \approx V_t + 2V_{ov}$$

- Systematic error is zero, since $V_{DS1} = V_{DS3}$

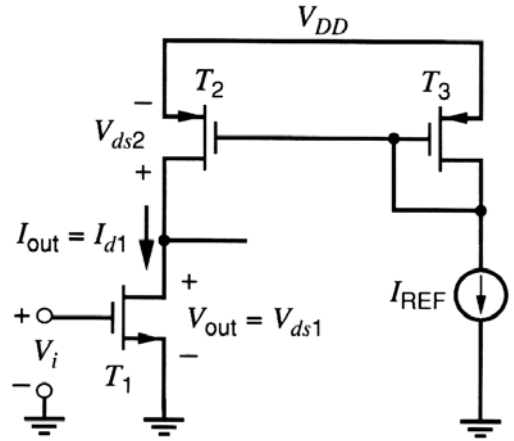


Active Loads

- To achieve a high gain
  - Need large load resistance
    - Difficult to realize resistor in an integrated circuit
    - But it is much cheaper/easier to use resistors => Active load
- Configurations
  - Common source with complementary load
  - Common source with diode load
  - Differential pair with current mirror load

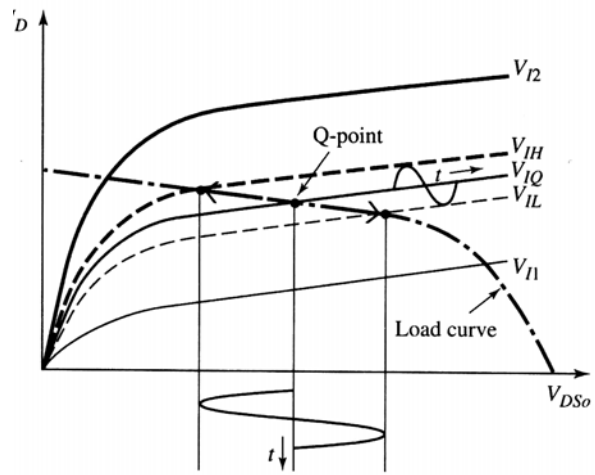
Common Source with MOS Load

- In this case, T2 operation is mostly defined by T3
- Output voltage is given by: $V_{OUT} = V_{DD} + V_{ds2}$



- In most part, the gain is not linear. But we can bias it in a narrow regime that gain stay constant for short channel devices

$$\frac{V_{OUT}}{V_{IN}} = -g_{m1}(r_{01} \parallel r_{o2})$$

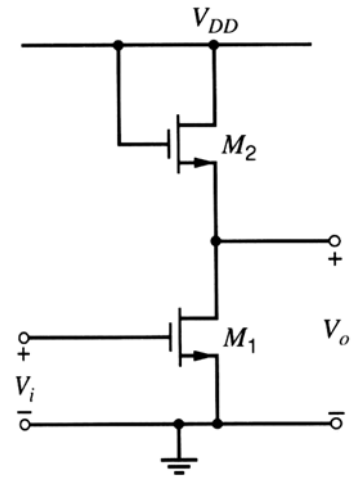


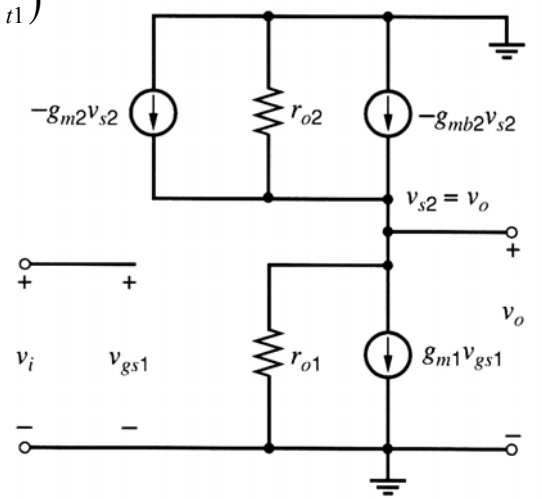
Common Source with Diode Connected Load

- In this case, the load resistance is proportional to $1/g_{m2}$
- Large signal analysis shows that the circuit is operational for
  - V_{in} greater than one threshold voltage
  - Vout could only goes to $(V_{DD}-V_{t2})$
- Small signal gain:

$$V_o = V_{DD} - V_{t2} - \sqrt{\frac{(W/L)_1}{(W/L)_2}}(V_i - V_{t1})$$

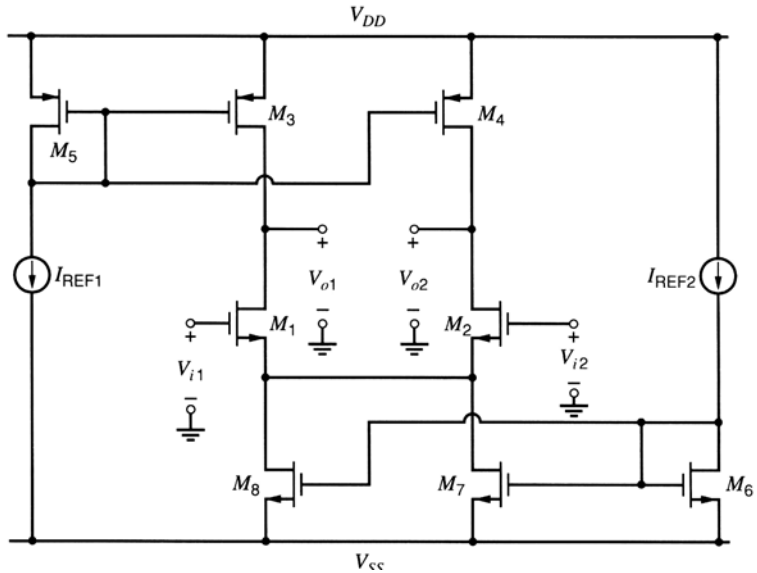
$$\frac{v_o}{v_i} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$





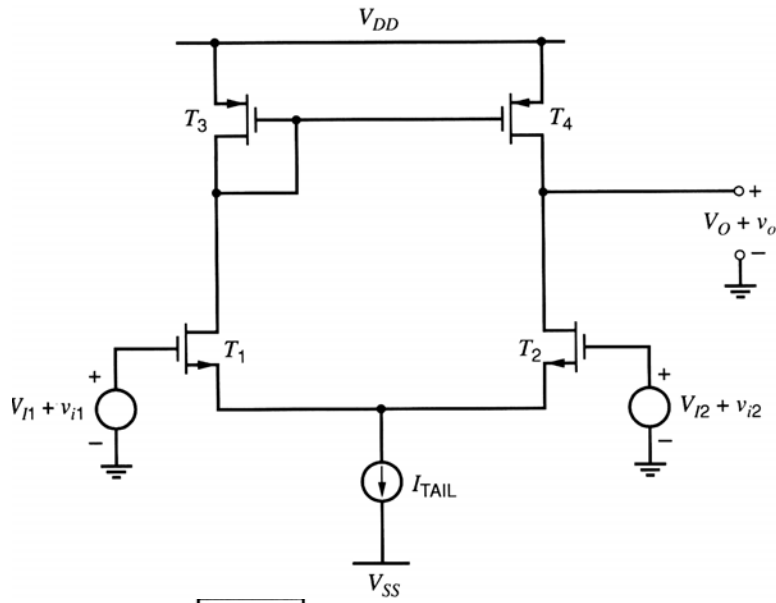
Differential Pair with Active Load

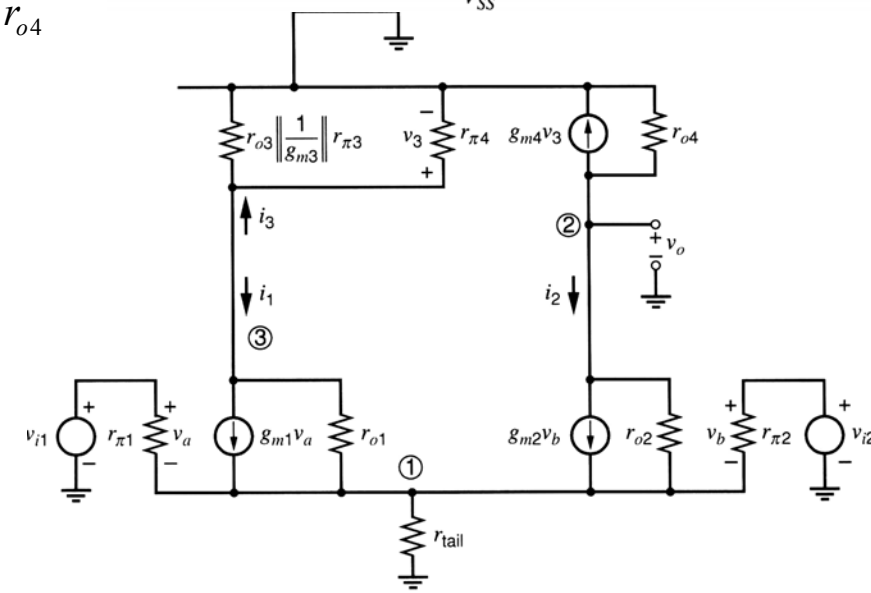
- Adding current mirror to differential pair, to achieve high differential gain
- Issue with this circuit: sensitive common-mode output voltage to change of drain currents
  - Reducing differential gain or range of outputs
- To avoid this problem, we need to adjust the sum of M_3 & M_4 to be equal to sum of M_7 & M_8



Differential Pair with Active Load (cont.)

- An alternative circuit is shown here:
  - Turning a differential pair into single ended
- Investigating small signal model shows the transconductance of actively loaded Diff-Pair is twice of resistively loaded $G_m = g_{m(dp)} = g_{m1}$
- The output resistance $R_o = r_{o2} \| r_{o4}$
  - Large output resistance, requires next stage also has a large input resistance
- Active load also improves CMRR by a factor of $2g_{m1}(r_{o2}||r_{o4})$



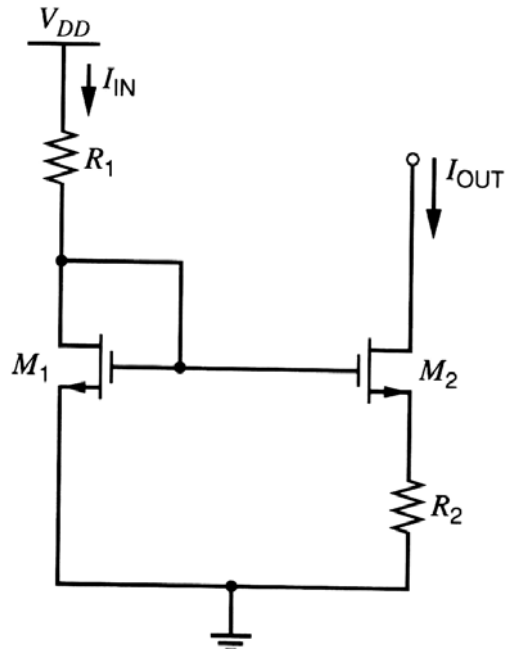


Voltage and Current Sources

- Low current biasing techniques for achieving small bias currents
  - Widlar current source
  - Peaking current source
- Supply insensitive biasing
  - Self biasing
- Temperature insensitive biasing
  - Band gap referenced circuit

Mos Widlar Current Sources

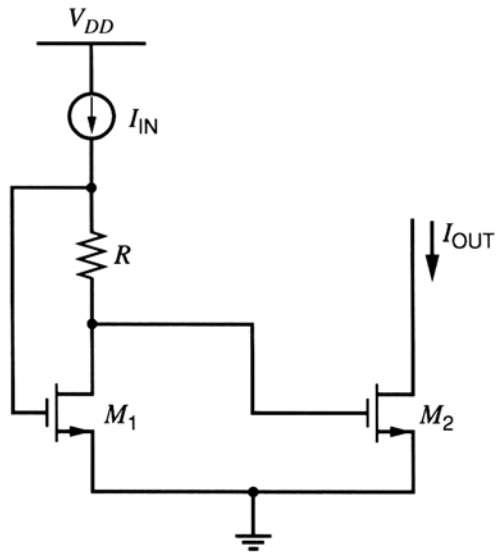
- Similar to Widlar current mirror, but addition of resistor makes output current less dependent of input current
- Output current depends on input current and resistor R_2



$$\sqrt{I_{out}} = \frac{-\sqrt{\frac{2}{k'(W/L)_2}} + \sqrt{\frac{2}{k'(W/L)_2} + 4R_2V_{ov1}}}{2R_2}$$

MOS Peaking Current Source

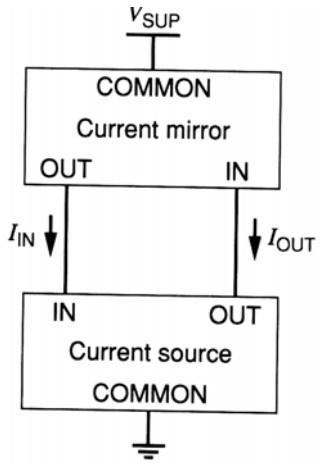
- To achieve even lower current values, the size of resistors will grow fast; alternatively we could use this class of circuits
- The output current is given;
  - In saturation: $I_{out} = \frac{k'(W/L)_2}{2}(V_{ov1} - I_{in}R)^2$
  - In sub-threshold: $I_{out} \approx I_{in} \exp\left(-\frac{I_{in}R}{nV_T}\right)$

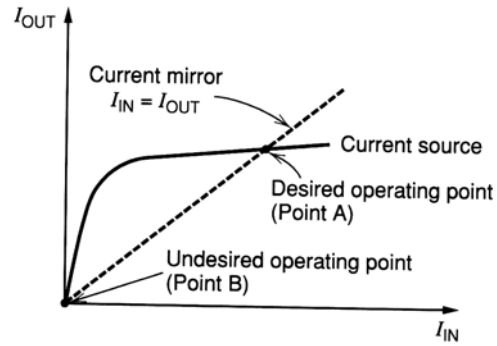


Supply Insensitive Biasing

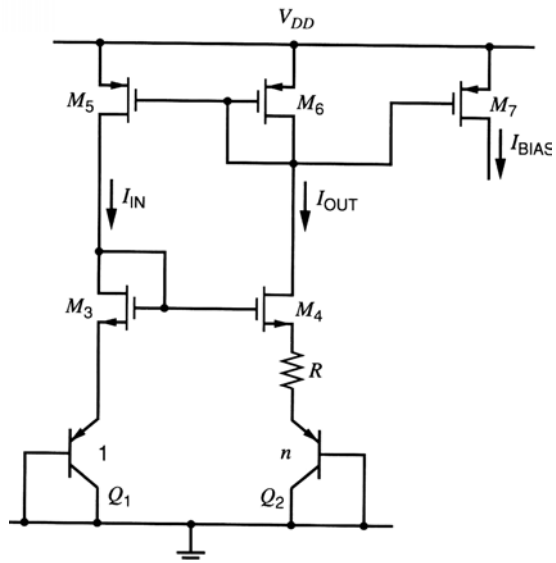
- An important aspect in a design is sensitivity to biases
  - Defined by:

$$S_{V_{SUP}}^{I_{OUT}} = \frac{V_{SUP}}{I_{OUT}} \frac{\partial I_{OUT}}{\partial V_{Sup}}$$





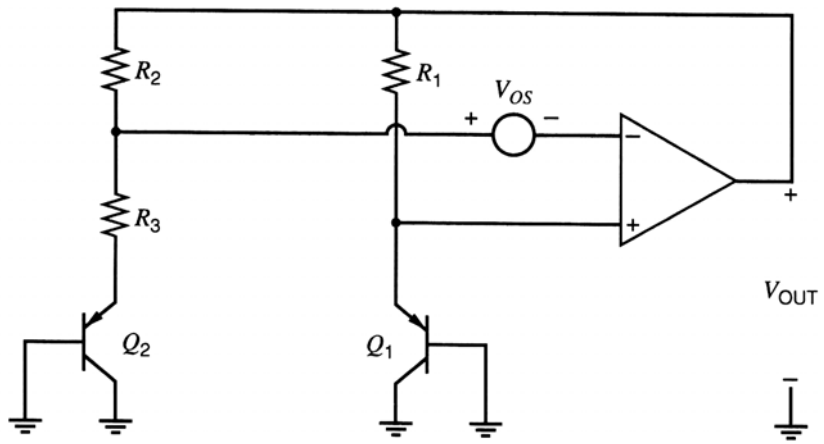
- Self biasing uses the concept of positive feedback; the input current is directly related to output current
- Needs an startup circuit to avoid zero current case
- A common approach is VT referenced self-bias circuit



$$I_{out} = V_T \frac{\ln(n)}{R}$$

Temperature Insensitive Biasing

- Designing temperature independent references
  - Band-gap referenced
- Using parasitic BJT in CMOS process, we can design band-gap referenced circuit



$$V_{out} = V_{EB2} + \left(1 + \frac{R_2}{R_3}\right)\Delta V_{EB} + \left(1 + \frac{R_2}{R_3}\right)V_{OS}$$

$$\Delta V_{EB} = V_T \ln\left(\frac{I_1 I_{S2}}{I_2 I_{S1}}\right)$$

Summary

- Sources and current mirrors
- Using active loads instead of plain resistors
- Temperature and bias insensitive circuits
- Practice questions: 4-5, 4-10, 4-12, 4-23, 4-25